WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a plurality of gate circuits; and

a control circuit configured to control the operation of some gate circuits among said plurality of gate circuits,

each of said some gate circuits among said plurality of gate circuits including:

a logic circuit constituted by a plurality of first transistors; and

a switch circuit which can switch whether a power supply voltage is supplied to said logic circuit, is constituted by a second transistor having a threshold voltage higher than that of said first transistor, and is controlled by said control circuit.

2. The semiconductor integrated circuit according to claim 1, wherein said some gate circuits are provided on a critical path.

3. A logic operation circuit comprising:

a gate circuit which is connected between a virtual voltage line and a first reference voltage line and constituted by a plurality of first transistors; and

a second transistor which is connected between a second reference voltage line and said virtual voltage line and constituted by a transistor having a threshold voltage higher than that of said first transistor,

a source/drain terminal of said first transistor in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit.

4. A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 3 is provided on a critical path.

Sub A3

5. A logic operation circuit comprising:

a gate circuit which is connected between a first reference voltage line and a virtual voltage line and constituted by a plurality of first transistors;

a second transistor which is connected between said virtual voltage line and a second reference voltage line and has a threshold voltage higher than that of said first transistor; and

a third transistor which is connected between said first reference voltage line and an output terminal of said gate circuit and has a threshold voltage higher than that of said first transistor,

said second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa.

Sub C1

6. The logic operation circuit according to claim 5, wherein a source/drain terminal of said first transistor in said gate circuit is connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit.

7. A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 5 is provided on a critical path.

Sub A4

Fig 6

8. A logic operation circuit comprising:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than said first transistor;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of said first transistor; and

a storage circuit capable of holding output logic of said

gate circuit,

said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit.

9. The logic operation circuit according to claim 8, wherein a source/drain terminal of said first transistor in said gate circuit is connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit.

10. A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 8 is provided on a critical path.

11. A logic operation circuit comprising:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than that of said first transistor;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of said first transistor; and

a bypass circuit which is connected to said gate circuit in parallel and constituted by a circuit substantially equal to said gate circuit by using a plurality of fourth transistors having a threshold voltage higher than that of said first transistor,

said bypass circuit being connected between said first and second reference voltage lines.

12. The logic operation circuit according to claim 11,

wherein a source/drain terminal of said first transistor in said gate circuit is connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate terminal.

13. A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 11 is provided on a critical path.

14. A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal, and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits being constituted by said logic operation circuits defined in claim 3,

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

15. A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and

an output terminal and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits being constituted by said logic operation circuits defined in claim 5,

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

16. A flip flop comprising:

a first conduction interception circuit capable of switching conduction or interception between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or interception between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit;

and a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits being constituted by said logic operation circuits defined in claim 8,

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

17. A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic

of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits being constituted by said logic operation circuits defined in claim 11,

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.